REMARKS

The following is in response to the Office Communication mailed on August 17, 2004, which required information related to the declaration of an interference and support for the pending claims. As noted in the Communication, claims 40-54 are respectively exact copies of claims 1-15 of U.S. patent number 6,525,986, of Prutchi *et al.* issued February 25, 2003. A two-column listing of the pending claims that applies each limitation or element of the pending claims to the disclosure of the application is given below. This is followed by a Request for Declaration of Interference, which is believed to provide the needed information.

SUPPORT FOR PENDING CLAIMS

The pending claims of present application, including the proposed Count 1, are primarily concerned with the "Device Select Scheme and Circuit" aspect of the present invention. This is primarily described in paragraphs [0016] and [0017] of the Summary and under section entitled "Device Select Scheme and Circuit", found in paragraphs [0062]-[0071], although additional details are provided in other sections. Particular attention is called to paragraphs [0069]-[0071].

References are to the clean version of the Substitute Specification submitted concurrently with the filing of the present application.

40. A method comprising:	Fig. 2A shows a plurality of chips (141), each connected to a pad (149), with an address code set by the connections 161, each of which are distinct. The address is sent to all chips along bus 135.
receiving an address at each of a plurality of memory chips, the plurality of memory chips including a first memory chip having a first programmable code and a second memory chip having a second programmable code, wherein the first programmable code is different from the second programmable code;	¶[0016], lns. 8-12: "When a memory chip is powered on, the address of the array as defined by the mount key is passed onto the device select circuit of the chip. To select a given memory chip, the correct array address for that chip is sent to all the chips in the array via the interconnecting serial bus.

	This address is compared at each chip with that it acquired from its each chips mount, and the chip that matched is selected or enabled by its device select circuit."
enabling the first memory chip based on a comparison of a portion of the received address with the first programmable code; and	¶[0069], lns. 9-11: "This output is clocked into the address-match register 307 [Fig. 5A] by the falling edge of CS* 171. This results in a S-R register 315 being set HIGH such that DS 309 is also HIGH and the device is selected."
disabling the second memory chip based on a comparison of the portion of the received address with the second programmable code.	¶[0069], lns. 11-12: "On the other hand, when the addresses do not match, DS 309 [Fig. 5A] will be LOW and the device is not selected."
41. The method of claim 40 wherein enabling the first memory chip based on a comparison of a portion of the received address with the first programmable code includes comparing two or more bits of the received address with the first programmable code.	¶[0016], lns. 3-14: "Each memory device chip has a multi-bit set of pinouts ..." See Fig. 5A for the connection of these pinouts at 147 being supplied to Comp 305.
42. The method of claim 40 wherein enabling the first memory chip based on a comparison of a portion of the received address with the first programmable code includes comparing the portion of the received address with a selection logic circuit.	¶[0069], lns. 7-8: "The comparator 305 [Fig. 5A] compares this address with that obtained from the device-select pinouts 147."

43. The method of claim 40 including comparing the portion of the received address with a first selection logic circuit of the first memory chip and with a second selection logic circuit of the second memory chip.	Each chip 141 has a Device Selection Circuit 203 (details Figs. 4 and 5A. The operation is described beginning at line 1 of paragraph [0069].
44. The method of claim 40 further comprising providing the address to a memory array of each of the plurality of memory chips.	¶[0016], lns. 9-11: "To select a given memory chip, the correct array address for that chip is sent to all the chips in the array via the interconnecting serial bus."
45. A method comprising: assigning a first selection code to a first memory chip and a second selection code to a second memory chip, wherein the second selection code differs from the first selection code; receiving a portion of an address at the first memory chip and at the second memory chip; comparing the portion of the address to the first selection code and to the second selection code; and enabling the first memory chip and disabling the second memory chip based on the comparison.	¶[0064], lns. 3-4: "the address for each location in the array is defined by the grounding configuration or "key" of the mount 149 thereat." ¶[0069], lns. 4-12: "a 5-bit array address is shifted into a shift register 311 from the serial-in lines ..." ¶[0069], lns. 7-8: "The comparator 305 [Fig. 5A] compares this address with that obtained from the device-select pinouts 147." ¶[0069], lns. 9-12: "This output is clocked into the address-match register 307 [Fig. 5A] by the falling edge of CS* 171. This results in a S-R register 315 being set HIGH such that DS 309 is also HIGH and the device is selected. On the other hand, when the addresses do not match, DS 309 [Fig. 5A] will be LOW and the device is not selected."

46. The method of claim 45 further comprising receiving the address at a first memory array of the first memory chip and at a second memory array of the second memory chip.	¶[0016], lns. 8-12: "When a memory chip is powered on, the address of the array as defined by the mount key is passed onto the device select circuit of the chip. To select a given memory chip, the correct array address for that chip is sent to all the chips in the array via the interconnecting serial bus. This address is compared at each chip with that it acquired from its each chips mount, and the chip that matched is selected or enabled by its device select circuit."
47. The method of claim 45 wherein assigning includes coupling a bonding pad to a voltage level.	¶[0064], lns. 3-4: "the address for each location in the array is defined by the grounding configuration or "key" of the mount 149 thereat." ¶[0049], lns. 2-4: "By selectively grounding certain pads, such as a pad 161 on the mount, each mount may be configured or "keyed" to designate a definite address of the array."
48. The method of claim 45 wherein assigning includes setting a programmable link.	¶[0017]: "The invention provides a simple scheme for assigning an array address to each of the chips mounted on a memory module's backplane..." ¶[0049], lns. 2-4: "By selectively grounding certain pads, such as a pad 161 on the mount, each mount may be configured or "keyed" to designate a definite address of the array."

49. The method of claim 45 wherein enabling the first memory chip and disabling the second memory chip based on the comparison includes enabling the first memory chip when the first selection code matches the portion of the address and disabling the second memory chip when the second selection code differs from the portion of the address.

¶[0069], lns. 4-12: ", a 5-bit array address is shifted into a shift register 311 from the serial-in lines SI0 237, SI1 239. The clocking signal is carried in by the control line P/D* 235 which is gate-enabled by a HIGH signal in the master chip select line CS* 171. The 5-bit array address is then passed from the shift register 311 via the bus 313 to the comparator 305. The comparator 305 compares this address with that obtained from the device-select pinouts 147. The comparator output 306 goes HIGH whenever the addresses match. This output is clocked into the address-match register 307 by the falling edge of CS* 171. This results in a S-R register 315 being set HIGH such that DS 309 is also HIGH and the device is selected. On the other hand, when the addresses do not match, DS 309 will be LOW and the device is not selected."

50. The method of claim 45 wherein assigning the first selection code to the first memory chip and the second selection code to the second memory chip includes assigning the first selection code to the first memory chip and separately assigning the second selection code to the second memory chip.

¶[0016], lns. 8-12: "When a memory chip is powered on, the address of the array as defined by the mount key is passed onto the device select circuit of the chip. To select a given memory chip, the correct array address for that chip is sent to all the chips in the array via the interconnecting serial bus. This address is compared at each chip with that it acquired from its each chips mount, and the chip that matched is selected or enabled by its device select circuit."

51. A method comprising:	Fig. 2A shows a plurality of chips (141), each connected to a pad (149), with an address code set by the connections 161, each of which are distinct. The address is sent to all chips along bus 135. The address lines are SI0 and SI1, as shown in Fig. 5A.
coupling a plurality of address lines of a first memory chip in parallel with a plurality of address lines of a second memory chip;	
setting a first code at the first memory chip;	¶[0064], lns. 3-4: "the address for each location in the array is defined by the grounding configuration or "key" of the mount 149 thereat."
receiving a portion of an address at the first memory chip;	¶[0069], lns. 4-12: "a 5-bit array address is shifted into a shift register 311 from the serial-in lines ..."
enabling the first memory chip if the received address portion matches the first code; and	¶[0069], lns. 9-11: "This output is clocked into the address-match register 307 [Fig. 5A] by the falling edge of CS* 171. This results in a S-R register 315 being set HIGH such that DS 309 is also HIGH and the device is selected."
otherwise disabling the first memory chip.	¶[0069], lns. 11-12: "On the other hand, when the addresses do not match, DS 309 [Fig. 5A] will be LOW and the device is not selected."
52. The method of claim 51 wherein enabling the first memory chip includes disabling the second memory chip.	¶[0069], lns. 9-12: "This output is clocked into the address-match register 307 [Fig. 5A] by the falling edge of CS* 171. This results in a S-R register 315 being set HIGH such that DS 309 is also HIGH and the device is selected. On the other hand, when the addresses do not match, DS 309 [Fig. 5A]

	will be LOW and the device is not selected."
53. The method of claim 51 further including coupling a plurality of data lines of the first memory chip in parallel with a plurality of data lines of the second memory chip.	See Fig. 2A or 2B. The chips 141 are connected in parallel to the bus 135.
54. The method of claim 51 further comprising setting a second code at the second memory chip independent of the first code.	¶[0016], lns. 8-12: "When a memory chip is powered on, the address of the array as defined by the mount key is passed onto the device select circuit of the chip. To select a given memory chip, the correct array address for that chip is sent to all the chips in the array via the interconnecting serial bus. This address is compared at each chip with that it acquired from its each chips mount, and the chip that matched is selected or enabled by its device select circuit."

REQUEST FOR DECLARATION OF INTERFERENCE

It is respectfully requested that an interference be declared between the present application and U.S. patent number 6,525,986, of Prutchi *et al.*, referred to below as the "`986 patent". Claims 40-54 of the present application are respectively exact copies of claims 1-15 of the `986 patent. Claim 45 of the present application, which is an exact copy of claim 6 of the `986 patent, is suggested as a first count for the interference, as follows:

Count 1

A method comprising:

assigning a first selection code to a first memory chip and a second selection code to a second memory chip, wherein the second selection code differs from the first selection code;

receiving a portion of an address at the first memory chip and at the second memory chip;

comparing the portion of the address to the first selection code and to the second selection code; and

enabling the first memory chip and disabling the second memory chip based on the comparison.

35 U.S.C. 135(b)

Claim 45of the present application was added by Preliminary Amendment, simultaneously with the filing of the present application on February 23, 2004. This is less than one year after the `986 patent was granted on February 25, 2003.

Effective Filing Date

As specified in the "Cross-Reference to Related Application" section, as amended by the Preliminary Amendment filed concurrently with the present application, of paragraph [0001] of the application, the present application is a continuation entitled to an effective filing date of July 26, 1991 due to the benefit of:

U.S. Application Serial No. 09/939,290, filed on August 22, 2001,

U.S. Application Serial No. 09/657,369, filed on September 8, 2000, now Patent No. 6,317,812,

U.S. Application Serial No. 09/064,528, filed on April 21, 1998, now Patent No. 6,148,363,

U.S. Application Serial No. 08/931,193, filed on September 16, 1997, now Patent No. 5,806,070,

U.S. Application Serial No. 08/396,488, filed on March 2, 1995,

U.S. Application Serial No. 07/736,733, filed on July 26, 1991, now Patent No. 5,430,859.

The `986 patent is shown to have a United States filing date of January 22, 2002, claiming priority from U.S. Application Serial No. 09/347,841, filed on July 2, 1999, now Patent No. 6,208,579, and from U.S. Application Serial No. 08/903,313, filed on July 30, 1997, now Patent No. 5,987,357. This over six years later than the July 26, 1991, effective filing date of the present application.

Therefore, it is requested that the interference be declared with the Applicants of the present application designated the senior party.

Claims Corresponding to the Proposed Count 1

The proposed Count 1 is an exact copy of claim 6 of the `986 patent. Claims 7-11 of the `986 patent are dependent on claim 6. Claims 1 and 12 of the `986 patent are also method claims, but written slightly differently and containing further limitations and can either be taken to correspond to claims which depend from claim 5, or serve as additional counts. Claims 2-5 of the `986 patent are dependent on claim 1, and claims 13-15 of the `986 patent are dependent on claim 12.

Support for the Proposed Count 1 in the Present Application

The pending claims of present application, including the proposed Count 1, are primarily concerned with the "Device Select Scheme and Circuit" aspect of the present invention. This is primarily described in paragraphs [0016] and [0017] of the Summary and under section entitled "Device Select Scheme and Circuit", found in paragraphs [0062]-[0071], although additional details are provided in other sections. Particular attention is called to paragraphs [0069]-[0071]. (References are again to the clean version of the Substitute Specification, submitted with the present application.)

Count 1	Present Application
45. A method comprising:	¶[0064], lns. 3-4: "the address for each location in the array is defined by the grounding configuration or "key" of the mount 149 thereat."
assigning a first selection code to a first memory chip and a second selection code to a second memory chip, wherein the second selection code differs from the first selection code;	
receiving a portion of an address at the first memory chip and at the second memory chip;	¶[0069], lns. 4-12: "a 5-bit array address is shifted into a shift register 311 from the serial-in lines ..."
comparing the portion of the address to the first selection code and to the second selection code; and	¶[0069], lns. 7-8: "The comparator 305 [Fig. 5A] compares this address with that obtained from the device-select pinouts 147."
enabling the first memory chip and disabling the second memory chip based on the comparison.	¶[0069], lns. 9-12: "This output is clocked into the address-match register 307 [Fig. 5A] by the falling edge of CS* 171. This results in a S-R register 315 being set HIGH such that DS 309 is also HIGH and the device is selected. On the other hand, when the addresses do not match, DS 309 [Fig. 5A] will be LOW and the device is not selected."

For these reasons, it is submitted to be clear that claim 6 of the `986 patent is supported by the present application disclosure, first filed on July 26, 1991.

`986 Patent Prosecution File History

A review of the file history of the `986 patent reveals that the material in the present application was cited neither during the `986 patent application process nor that of its parents.

Information Disclosure Statement

An Information Disclosure Statement and accompanying forms 1449 are being prepared in order to cite references cited in the '986 patent and its parents and should be submitted within the next few weeks. As soon as copies of the non-patent reference are obtained, the Information Disclosure Statement will be submitted.

Conclusion

It is believed that the above provides the information required by the Communication. A prompt declaration of the requested interference is respectfully requested. In the meantime, however, if the Examiner has any questions about this request, application or disclosure statements, a telephone call to the undersigned is invited.

Respectfully submitted,

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